Claims

What is claimed is:

Claim 1

1. For use in a data processing system having a memory coupled to multiple requesters, a memory coherency system, comprising:

a memory circuit coupled to provide a copy of requested data from the memory to a first requester, and to initiate invalidation operations to invalidate all read-only copies of the requested data that are stored by one or more other requesters; and

a circuit included within the first requester and responsively coupled to the memory circuit to execute an instruction that causes the first requester to temporarily enter a stalled state until all of the invalidation operations have been completed.

Claim 2

2. The system of Claim 1, wherein the data is provided before the invalidation operations are completed.

Claim 3

3. The system of Claim 2, wherein the memory circuit includes a request channel and a response channel.

Claim 4

4. The system of Claim 3, wherein the memory circuit includes an acknowledge tracker to initiate the transfer of an acknowledge to the first requester when all invalidation operations for the requested data are completed.

Claim 5

5. The system of Claim 4, wherein the requester includes a request tracking circuit responsively coupled to the memory to record when the acknowledge is outstanding for the requested data.

Claim 6

6. The system of Claim 1, wherein the first requester issues multiple requests, and wherein the circuit prevents any further instruction processing from occurring within the first requester until all invalidation operations have been completed for all of the multiple requests.

Claim 7

7. The system of Claim 6, wherein the first requester is a processing node that includes multiple processors, wherein the circuit resides within one of the multiple processors and includes logic to execute an instruction to stall the processor until all of the invalidation operations have been completed for data previously provided to the processor.

Claim 8

8. The system of Claim 6, wherein the first requester is a processing node that includes multiple processors, wherein the circuit resides within one of the multiple processors and includes logic to execute an instruction to stall the processor until all of the invalidation operations have been completed for data previously provided to predetermined ones of the processor in the processing node.

Claim 9

9. For use in a system having multiple requesters coupled to a shared memory, a method for controlling processing of requests, comprising:

a.) issuing a request for data by a requester to the shared memory;

b.) providing the data from the shared memory in response to the request before all read-only copies of the data retained by other requesters have been invalidated; and

c.) stalling the requester until all of the read-only copies have been invalidated.

Claim 10

10. The method of Claim 9, wherein step c.) includes the initiation by the requester of a hardware sequence to stall the requester until the read-only copies have been invalidated.

Claim 11

11. The method of Claim 10, wherein the requester is an instruction processor, and further including execution of a predetermined instruction to initiate the hardware sequence.

Claim 12

12. The method of Claim 11, wherein the instruction is part of the hardware instruction set of the instruction processor.

Claim 13

13. The method of Claim 9, and including repeating steps a.) and b.) for multiple requests, and stalling the requester until all read-only copies of any data requested by any of the multiple requests have been invalidated.

Claim 14

14. The method of Claim 9, wherein the requester is a processing node containing multiple processors, and wherein the method comprises:

a.) issuing a request for data by one of the processors to the shared memory;

b.) providing the data from the shared memory to the processor in response to the request before all read-only copies of the data retained by other requesters have been invalidated; and

c.) stalling the processor until all of the read-only copies have been invalidated.

Claim 15

15. The method of Claim 14, wherein a.) and b.) are repeated for multiple requests, and wherein step c.) includes stalling the processor until all read-only copies of any data previously provided to the processor have been invalidated.

Claim 16

16. The method of Claim 15, wherein steps a.) through c.) may be performed for more than one processor in the processing node, and wherein step c.) comprises stalling a processor until all read-only copies of any data previously provided to the processor have been invalidated.

Claim 17

17. The method of Claim 15, wherein steps a.) through c.) may be performed for more than one processor in the processing node, and wherein step c.) comprises stalling a processor until all read-only copies of any data previously provided to predetermined ones of the processors in the processing node have been invalidated.

Claim 18

18. The method of Claim 9, and further comprising issuing an inter-processor interrupt by the requester to another requester to indicate that data stored within the shared memory by the requester may be accessed by the other requester.

Claim 19

19. A system for use in managing requests within a data processing system, comprising:

means for providing data in response to a request before all read-only copies of the data that reside within the data processing system at the time of receipt of the request have been invalidated; and

means for selectively discontinuing predetermined data processing tasks until all of the read-only copies have been invalidated.

Claim 20

20. The system of Claim 19, wherein the data processing system includes a shared main memory coupled to multiple instruction processors, and wherein the means for selectively stalling includes means provided within at least one of the instruction processors for executing a predetermined instruction to stall the at least one instruction processor.

Claim 21

21. The system of Claim 20, wherein the means for executing includes means for stalling the respective instruction processor until all read-only copies of any data that was previously requested by the instruction processor have been invalidated.

Claim 22

22. The system of Claim 21, wherein execution of the predetermined instruction by a instruction processor issues a request for data, and wherein the means for selectively stalling includes request tracking means for delaying return of the data until all read-only copies of any data that was previously requested by the instruction processor have been invalidated.